

# Accelium™ 4000 Coprocessors

Product Overview



Delivering ultra-high throughput and low latency the DRC PCIe Accelium™ coprocessors support the most demanding of complex applications. Optimized for big data indexing, search and analytics the coprocessors easily integrate into existing application data flows using the DRC Milano™ environment. Executing compute intensive routines the coprocessors can achieve 100 times acceleration versus software.



DRC Accelium Accelerator

**DRC Accelium coprocessors** combine the most advanced FPGAs with DRC technology that provides easy integration and programming of the coprocessor - the DRC Milano™ environment. This patented IP ensures that computationally complex routines are executed at maximum performance yet are integrated into the application as subroutine calls requiring no application source code changes.

The DRC Accelium PCIe coprocessors deliver:

- The highest performance coprocessor using the Xilinx UltraScale™ FPGAs
- Acceleration factors up to 100 times a CPU
- Internal memory bandwidth in excess of 10 TB/s
- Full PCIe Gen 3 support at up to 256 Gbps
- DDR4 memory support
- Reconfigurable in < 200 msec
- Very low power with typical power consumption of 25 watts per FPGA

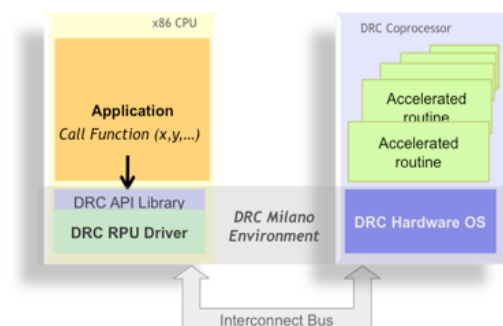
The DRC Accelium coprocessor is a patented, ultra-high performance engine that executes complex data manipulation routines using massively parallel structures.

DRC coprocessor routines are available to co-resident software based applications through the DRC API.

Tightly coupling the Accelium coprocessor with a CPU delivers very low latency, ultra-high data bandwidth to the most demanding applications. Architected for applications that are sub-second time- critical and that process gigabytes of data the Accelium coprocessor delivers unprecedented performance.

Accelium coprocessors use process pipelining and replication in its massively parallel architecture. Further advantages are achieved with the ability to right-size operators to any data width and to utilize multi-input operators, frequently reducing iterative processes to single cycle operations.

## The DRC Milano environment



The DRC Milano environment integrates the Accelium coprocessor with the CPU to provide a user-friendly application support environment. Milano is a sophisticated, low overhead operating environment.

With API, driver and management interface on the CPU, and a hardware operating system on the DRC coprocessor the following realtime functions are provided:

- DMA and PCIe bus arbitration management
- Very low overhead and low latency paths
- Coprocessor resource arbitration management
- Run Time Reconfiguration
- In-field upgradeable
- Set of well behaved, consistent interfaces
- Full Linux support

## The DRC Difference

With over 200 man-years of experience in developing low latency, high capacity solutions DRC has a unique talent in accelerated big data applications.

By utilizing a task based architecture DRC has optimized data management/data analysis balance. The key to achieving ultra-high performance is distributing processing capacity so that's its available where its needed rather than centralizing it. Moving the processing to the data versus the data to the processor.

## Made in America

DRC is a US based company with all staff US citizens, and all its engineering and product sourcing conducted in the US.

Accelium AC4000		
FPGA	AC4750	AC4950
Xilinx UltraScale	KU115	XCVU190
Logic Elements	1,451,000	2,350,000
Registers	663,360	2,148,480
Memory BRAMs	75.9 Mb	132.9 Mb
Physical/Mechanical		
Bus	PCIe Gen 3 x 16	PCIe Gen 3 x 16
Dimensions	4.38" x 9.5"	4.38" x 9.5"
Power	Typical 25W	Typical 25W
Memory		
DDR4 SDRAM	2 x 4GB	4 x 4GB Micron HMC
Comm		
QSFP+	0	2 x 40Gbps

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